

nForce 680i and 680a

NVIDIA's Next Generation Platform Processors

Agenda



- Platform Overview
- System Block Diagrams
- C55 Details
- MCP55 Details
- Summary

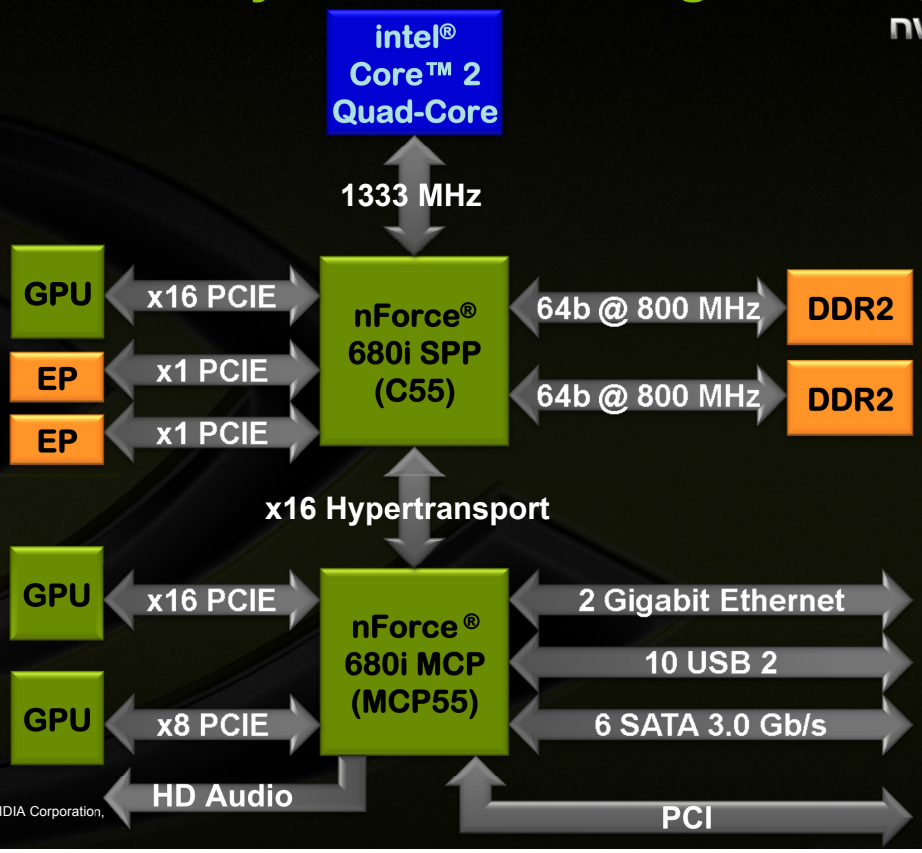
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Platform Overview

- nForce 680i
 - For systems using the Intel Core Duo processor
 - Implemented with the C55 and MCP55
 - Support for Dual Core and Quad Core Processors
- nForce 680a
 - For systems using AMD Athlon64 FX processors
 - Implemented with a pair of MCP55s
 - Support for 1 or 2 Dual Core Processors
- Both
 - Sufficient PCIE lanes to enable Multi-GPU rendering (SLI) and have a GPU dedicated to physics

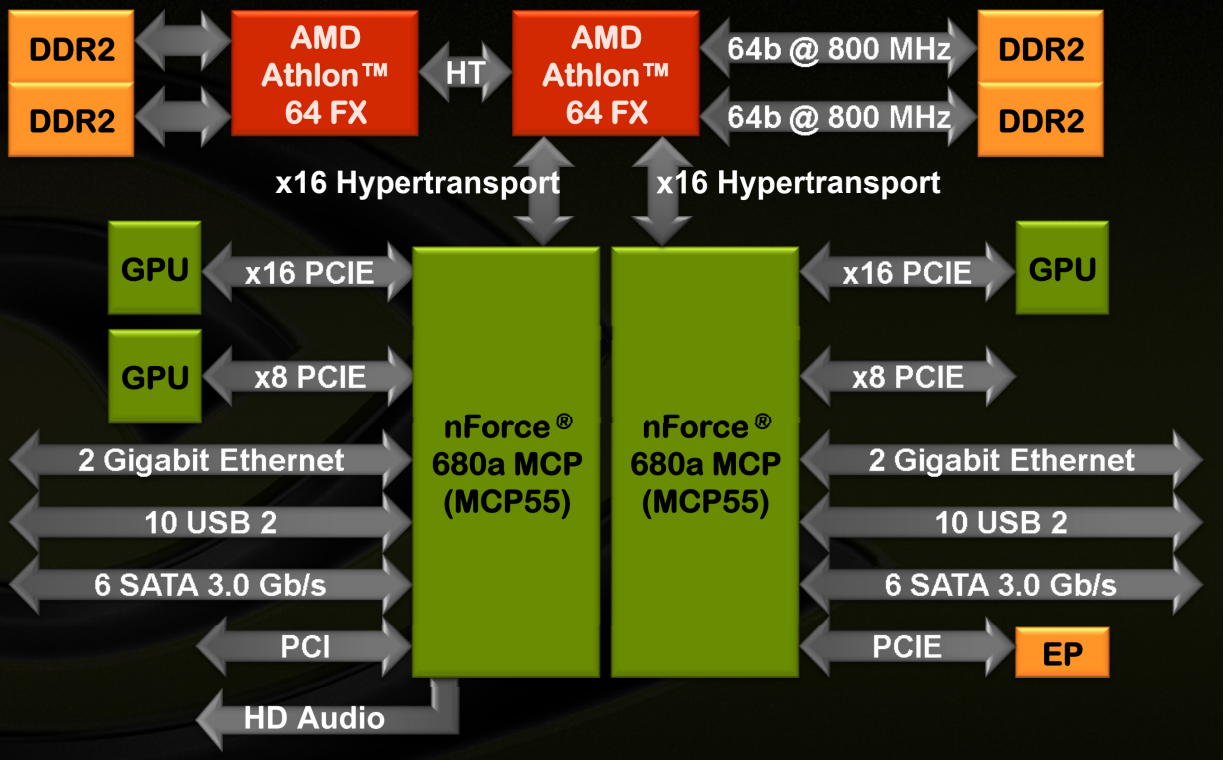
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nForce® 680i System Block Diagram



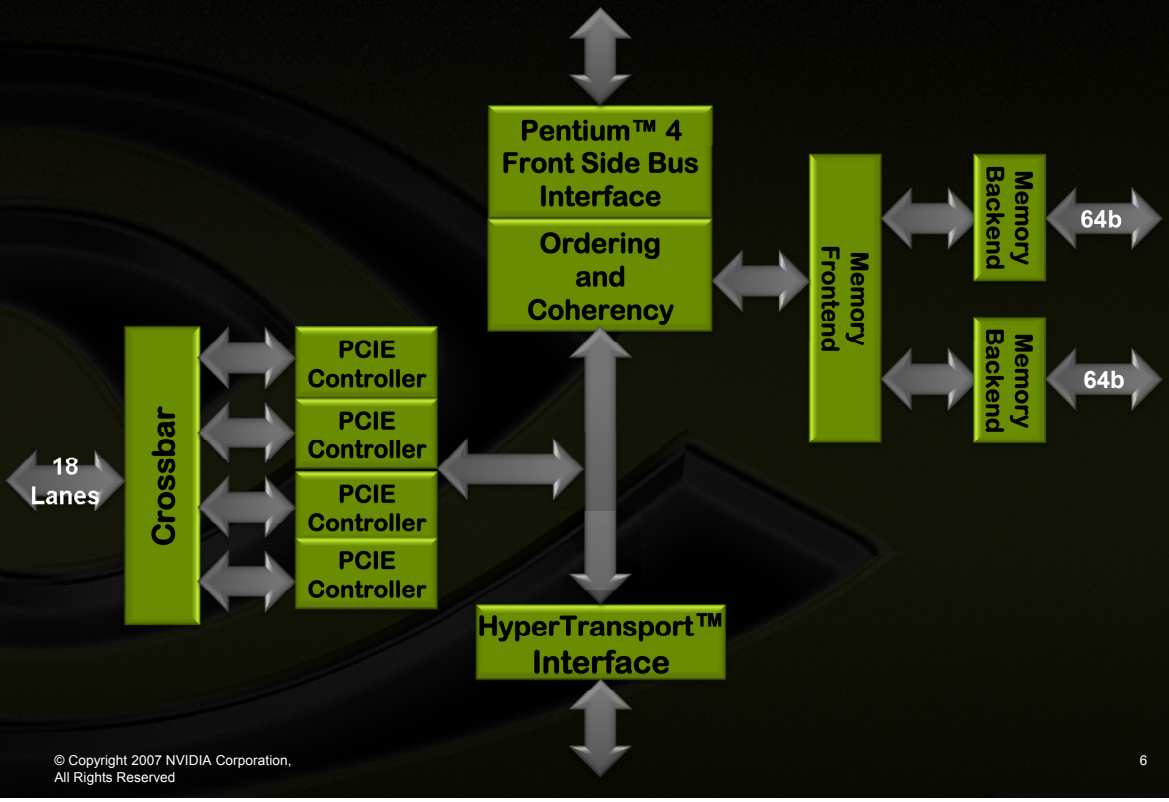
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nForce® 680a System Block Diagram



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C55 Block Diagram



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C55 Interfaces

- Core 2 Duo FSB
 - 1333 MHz
 - Support for both Dual and Quad Core Processors
- Memory Interface
 - 128 bit wide memory channel
 - Two 64 bit channels ganged together
 - DDR2 up to 800 MHz
- PCIE
 - 18 Lanes
 - 4 Controllers
 - Supports both x16-x1-x1 and x8-x8-x1-x1 configurations

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C55 Performance Features

- FSB and Memory Interface Overclocked Independently
 - FSB up to 2100 MHz
 - Memory Interface up to 1200 MHz
- Support for Enhanced Performance Profiles (EPP)
 - Extension of Serial Presence Detect (SPD)
 - Provides additional information to automatically set the voltage and timing parameters out of spec for overclocking configurations
- Advanced Prefetching

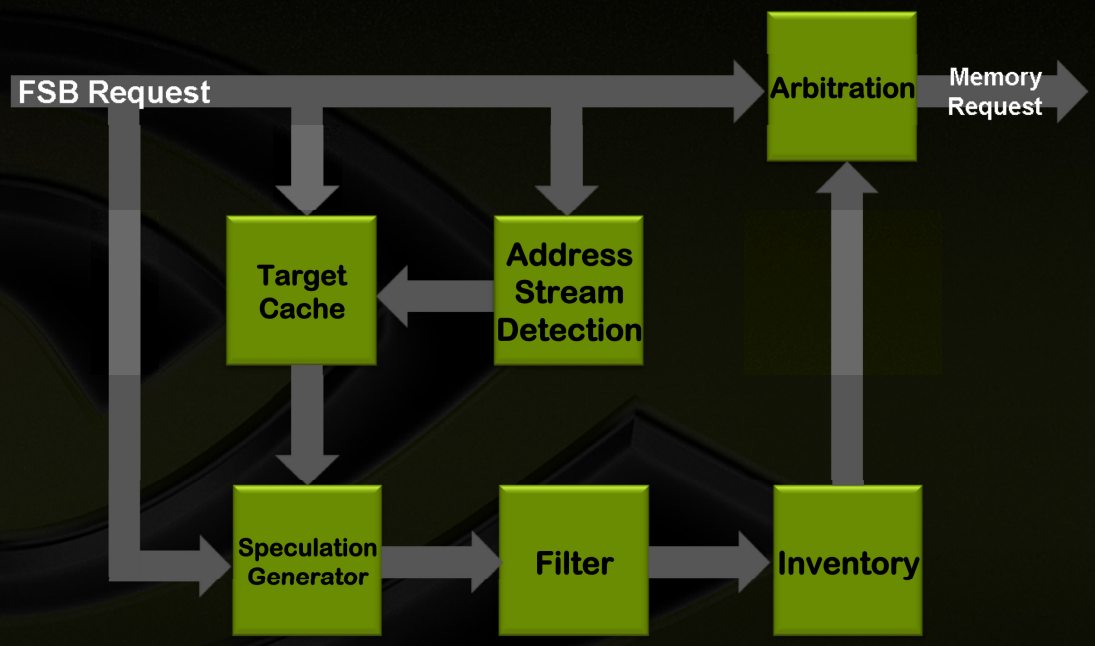
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Prefetcher

- Located in the Memory Front End
- Contains Multiple Algorithms
- Algorithms Run Concurrently
- Filter Prevents Prefetcher Swamping Memory Subsystem

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Prefetcher Block Diagram



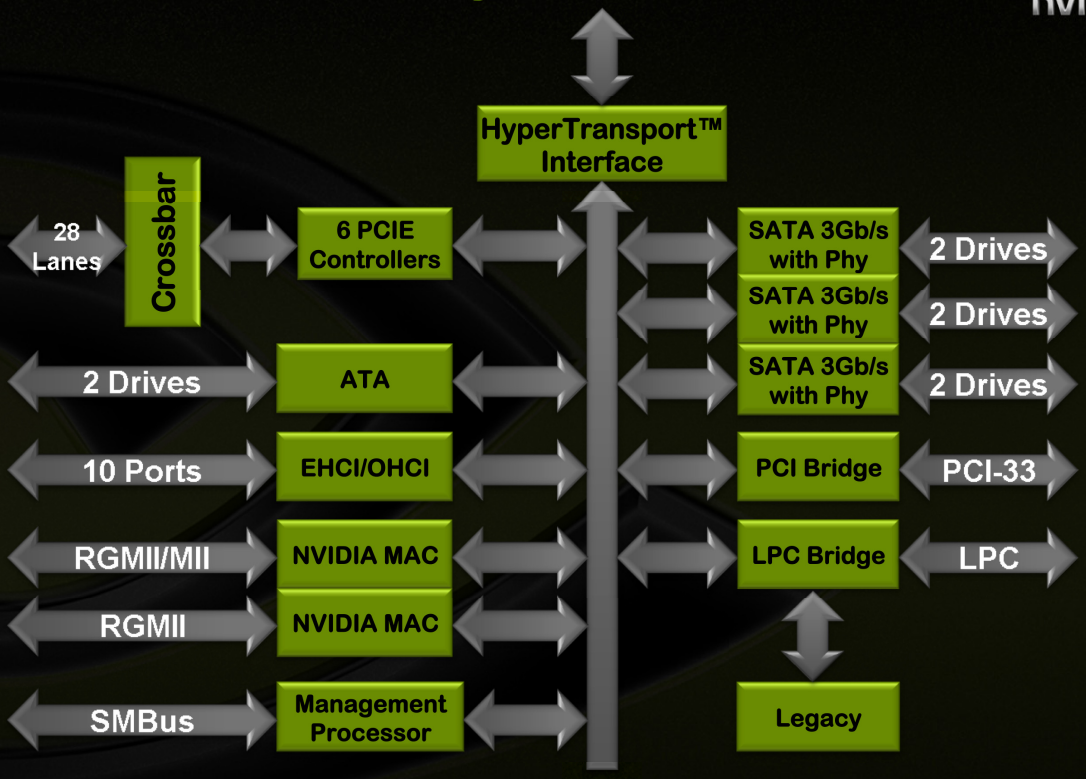
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C55 Stats

- Die
 - 10.21 mm x 7.64 mm
 - 90 nm Process
 - 51.2 Million transistors
- Package
 - 33 x 33 mm
 - 1212 balls @ 0.8 mm pitch
 - 8 layer substrate

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MCP55 Block Diagram



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MCP55 Interfaces

- Hypertransport
 - x16
 - 1GHz
 - Connects to either the C55 or Athlon64 FX
- PCIE
 - 28 Lanes
 - 6 Controllers
 - Multiple Configurations
- 2 Gigabit Ethernet MACs
- 6 Serial ATA 3.0 Gigabit/s ports
- 10 USB 2.0 ports

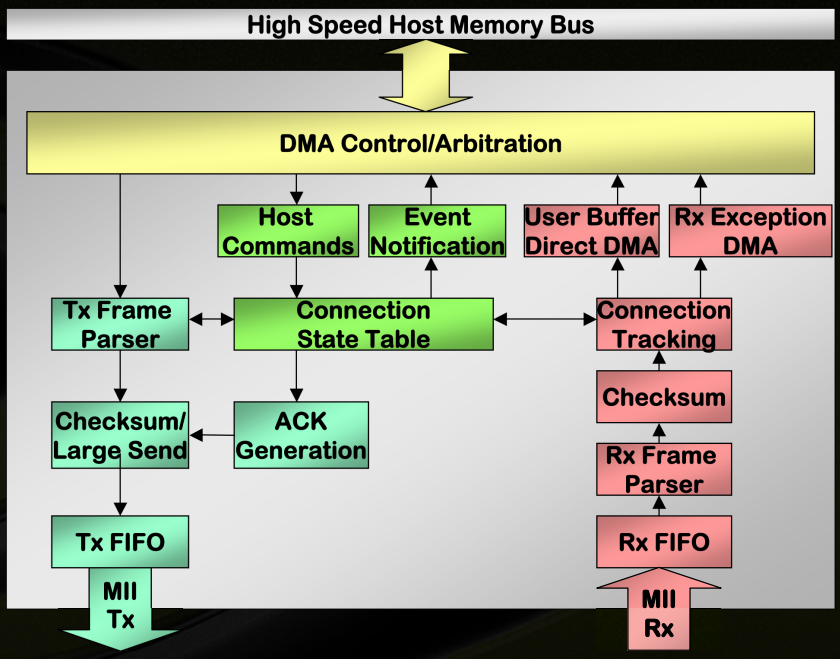
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MCP55 Networking

- TCP/IP Offload
- Ganging
 - Both MACs can be used as a single logical connection
- QOS
 - Packets from particular applications can be given priority
 - Typical usage is to keep latency low for online game in the face of a bulk data transfer

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Hardware Offload of TCP/IP



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MCP55 Stats

- Die
 - 8.69 mm x 12.05 mm
 - 140 nm Process
 - 50.8 Million Transistors
- Package
 - 33 x 33 mm
 - 776 balls @ 1 mm pitch
 - 6 layer substrate

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Supporting both Intel and AMD Platforms

- MCP55 performs power sequencing for entire system
- MCP55 sequences reset for everything except the processor in the 680i platform
- C55 sequences the reset for the processor in 680i systems
- C55 acquires the proper FSB voltage and frequency from the Boot ROM
- Interrupts
 - MCP55 converts APIC interrupts into HT format for delivery to either the Athlon64 or the C55
 - In 680i systems the C55 converts the interrupt to the FSB format

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Summary

- The nForce 680i and 680a Provide the Core for Enthusiast Systems Containing both Intel and AMD Processors
- Robust Performance is Provided with
 - Multi-GPU support
 - Flexible overclocking
 - Sophisticated prefetch
 - TCP/IP offload

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